Nanocrystal embedded MOS non volatile memory devices

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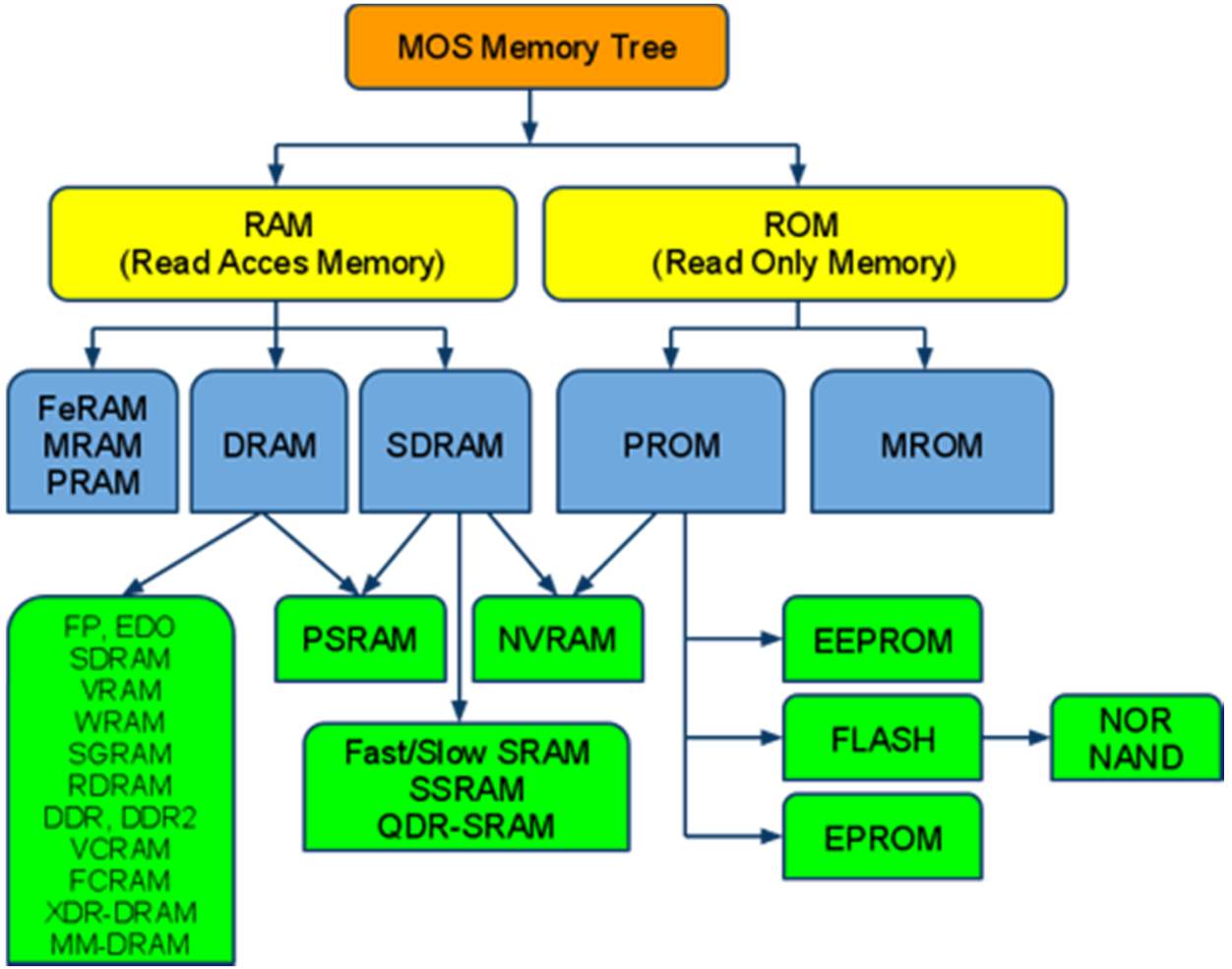
Various MOS Memory Devices



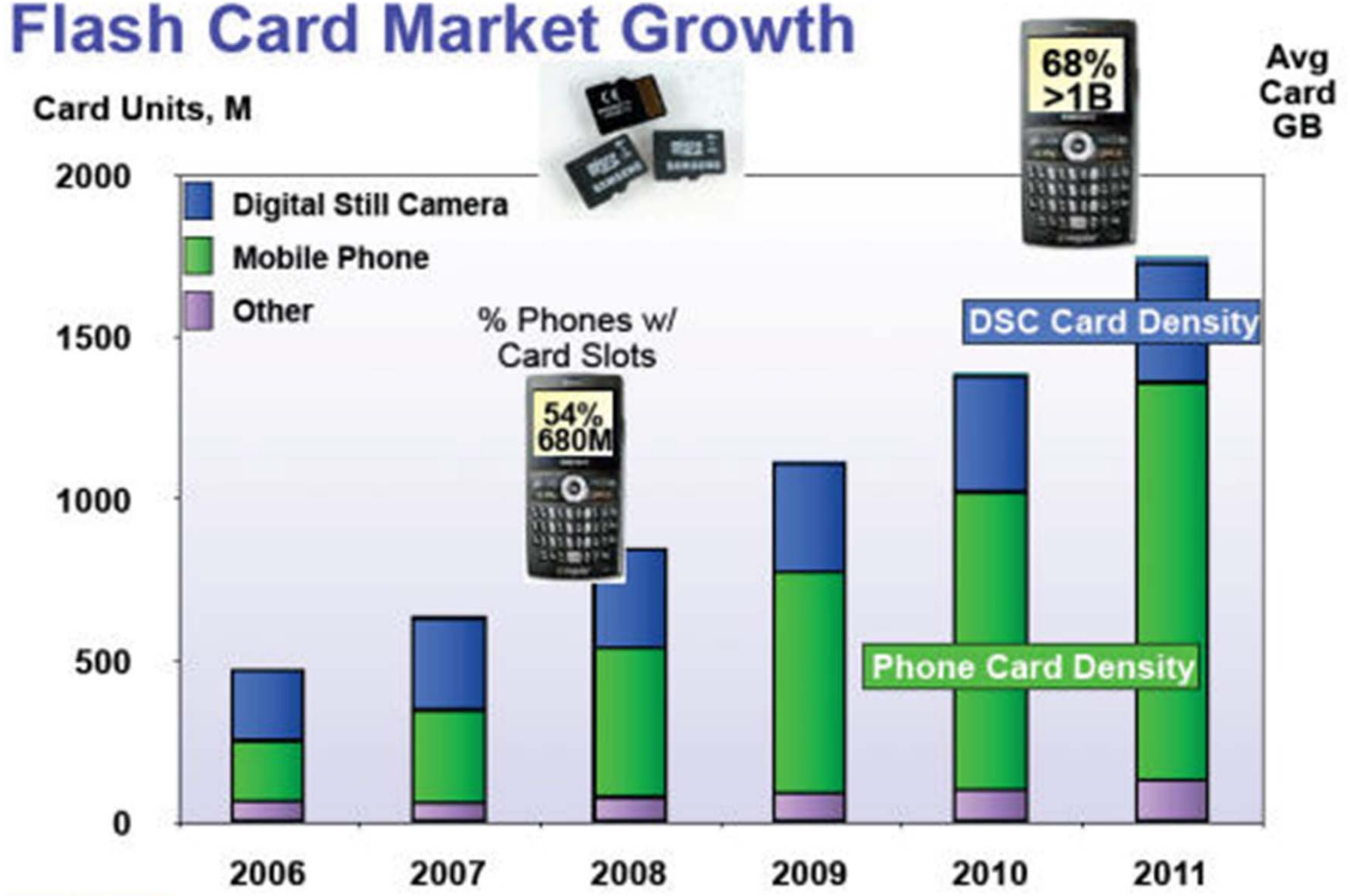
(Source: *www.sdram-technology.info/**MOS-MemoRY-Tree**.HTML*)

Applications of MOS Memory Devices

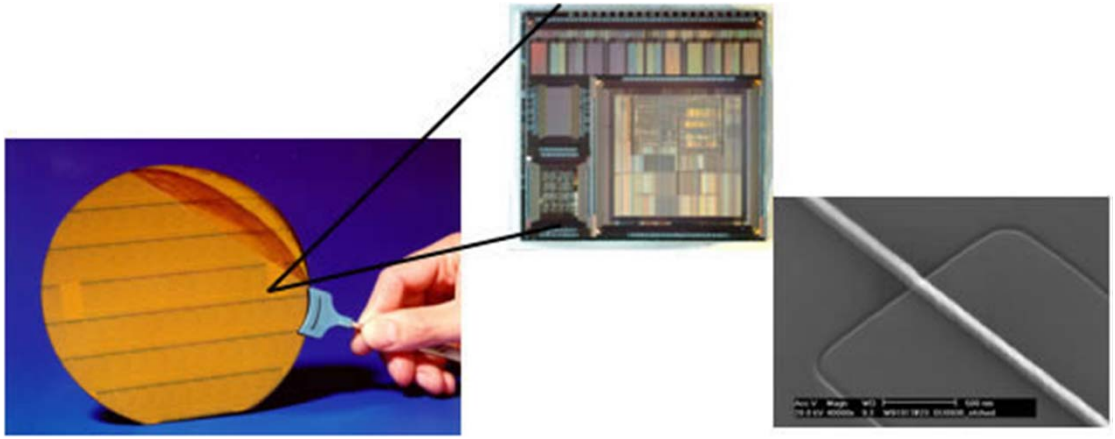
- ✓USB Flash drives
- ✓Memory cards (SD,MMC,M2) used in mobile phones, digital cameras, MP3 players
- ✓Computer DRAMs, Solid State Hard Drives (HDD)

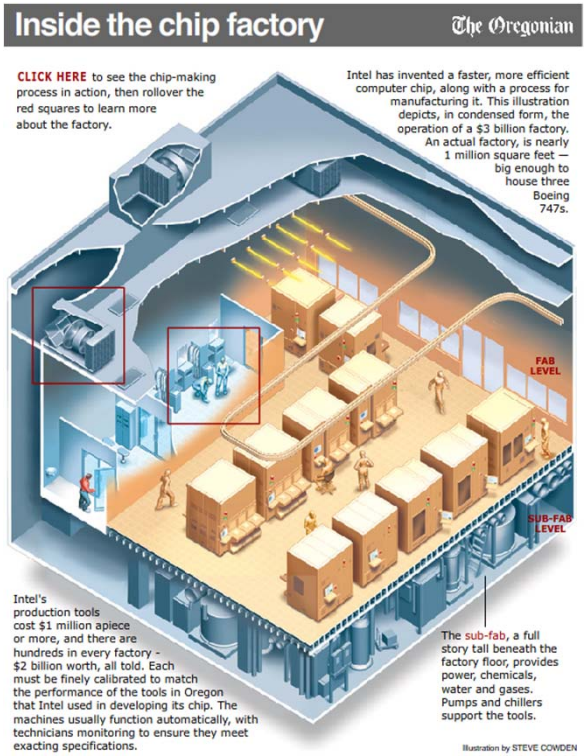
& many more

Flash Card Market Growth

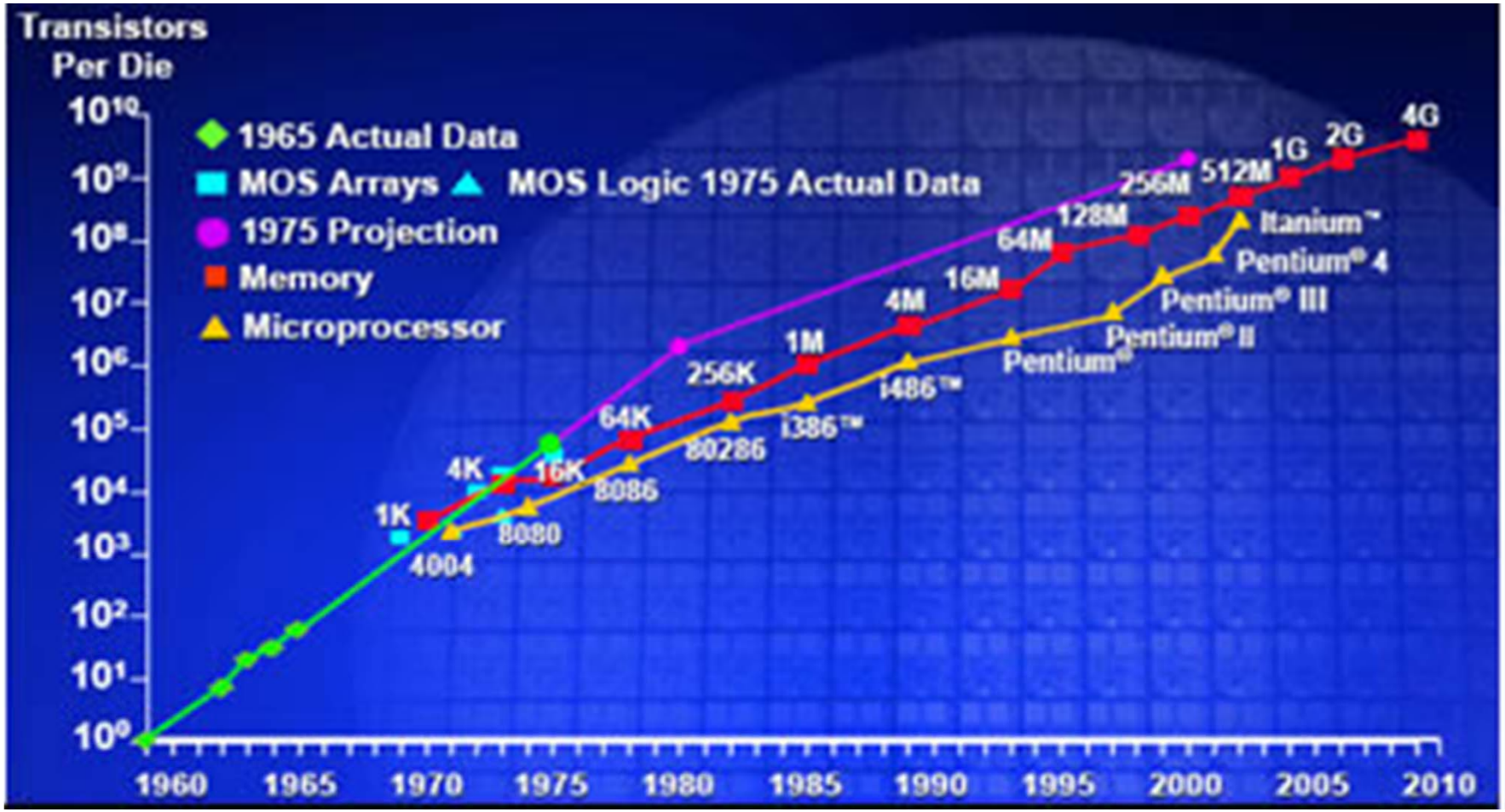


*Source : SEC Marketing

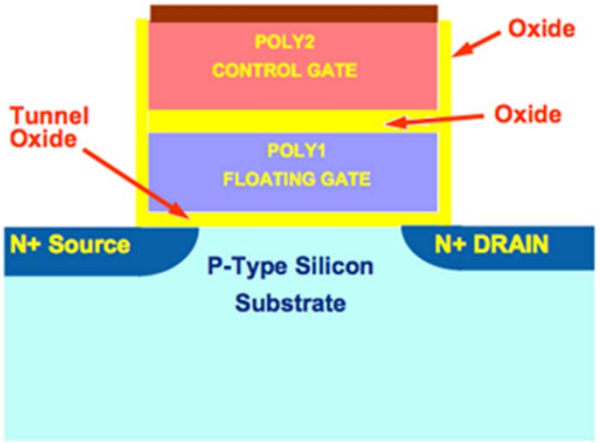



Inside the chip factory
The Oregonian
CLICK HERE to see the chip-making process in action, then rollover the red squares to learn more about the factory.
Intel has invented a faster, more efficient computer chip, along with a process for manufacturing it. This illustration depicts, in condensed form, the operation of a $3 billion factory. An actual factory, is nearly 1 million square feet — big enough to house three Boeing 747s.
FAB LEVEL
SUB-FAB LEVEL
Intel's production tools cost $1 million apiece or more, and there are hundreds in every factory - $2 billion worth, all told. Each must be finely calibrated to match the performance of the tools in Oregon that Intel used in developing its chip. The machines usually function automatically, with technicians monitoring to ensure they meet exacting specifications.
The sub-fab, a full story tall beneath the factory floor, provides power, chemicals, water and gases. Pumps and chillers support the tools.
Illustration by STEVE COWDEN

Transistors per die of MOS Memory Devices

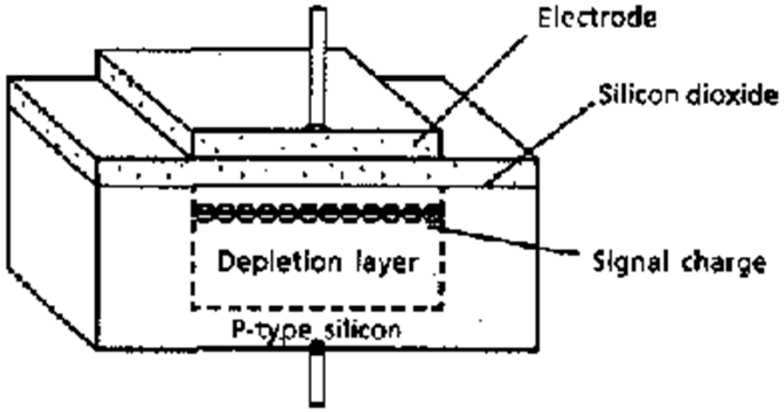


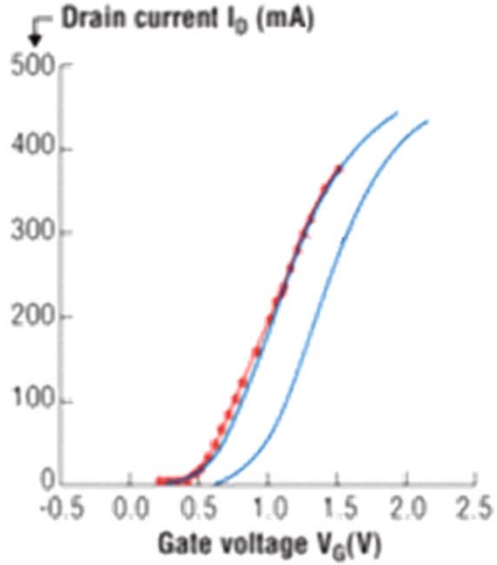
MOSFET memory and MOS capacitors



MOSFET memory devices rely on charge stored in the Floating Gate to cause a shift in the threshold voltage.

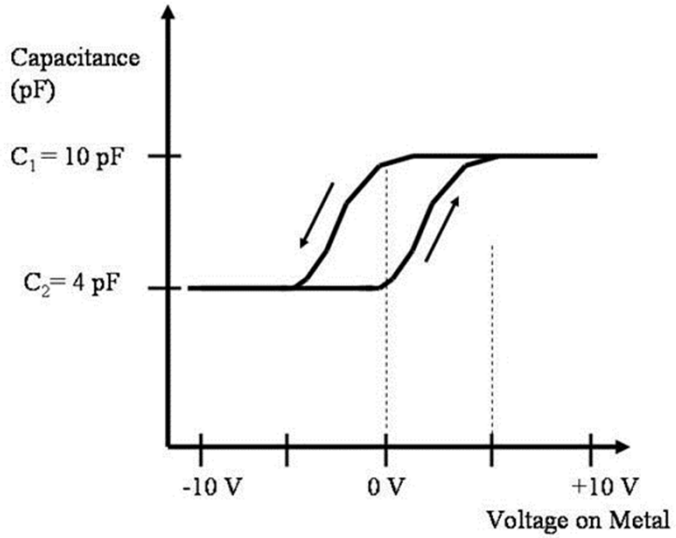
MOS Capacitors also act as memory devices



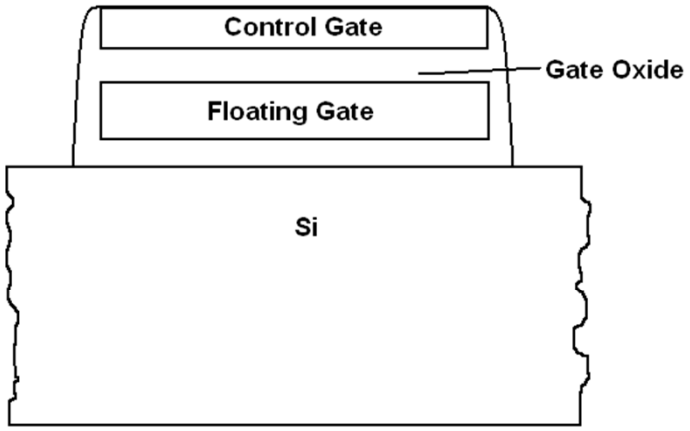


MOSFET memory and MOS capacitors

MOS capacitors rely on the Flatband Voltage Shift due to charge stored in the Floating gate (for FGMOS) or Oxide-Nitride layer(for SONOS).



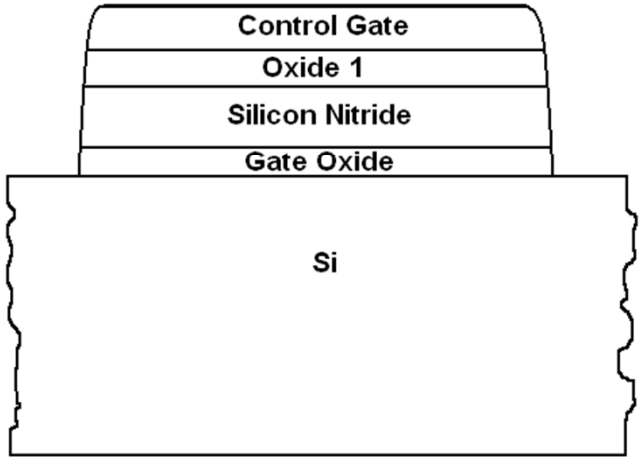
Some MOS Memory Devices: Capacitors



Floating Gate MOS memory device

✓Charges are stored in the polysilicon Floating Gate.
✓Most commonly used for Flash memory applications.

✓Charges are stored in the Oxide-Nitride interface.
✓Another variant MNOS useful for Aerospace/Military applications.

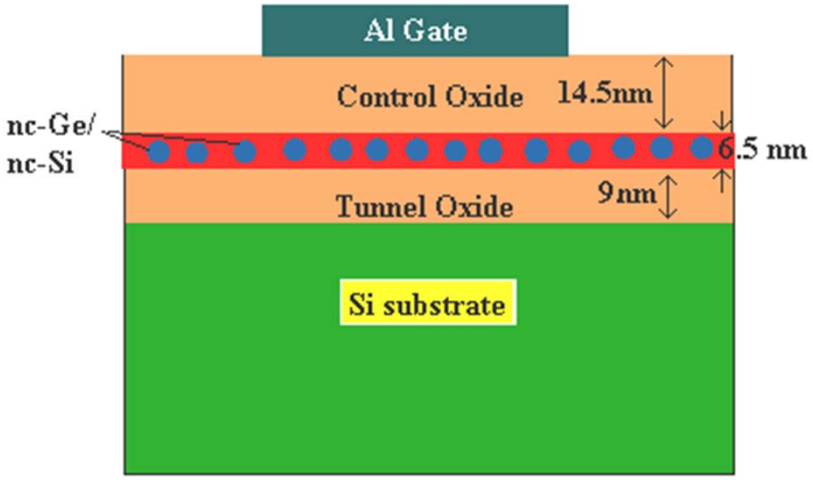


SONOS MOS memory device

Disadvantage of conventional MOS Memory Devices

- With scaling and thinner tunnel oxides, leakage provides a major challenge.
- Also for portability lesser write voltages are required.
- Advantages of Nanotechnology may be applied to MOS devices.
- Nanocrystal embedded MOS NVMs can help in this regard.

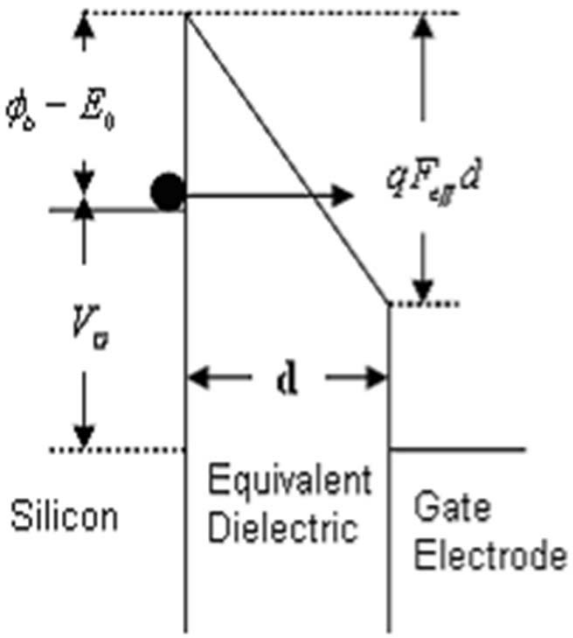
Nanoparticles Based Floating Gate MOS Memory Structure



Nanoparticles embedded floating gate

- Nanoparticles(nc) diameter in 5-6nm range.
- Confined in a narrow layer within SiO_2 called embedded gate dielectric
- Charging and discharging of nc carried out by electron tunneling
- Electrons tunnel from Si substrate to gate electrode through gate dielectric
- A thin tunneling barrier is formed at the interface of silicon substrate and composite gate dielectric
- Comparison of nc-Si and nc-Ge embedded gate oxide MOS devices.

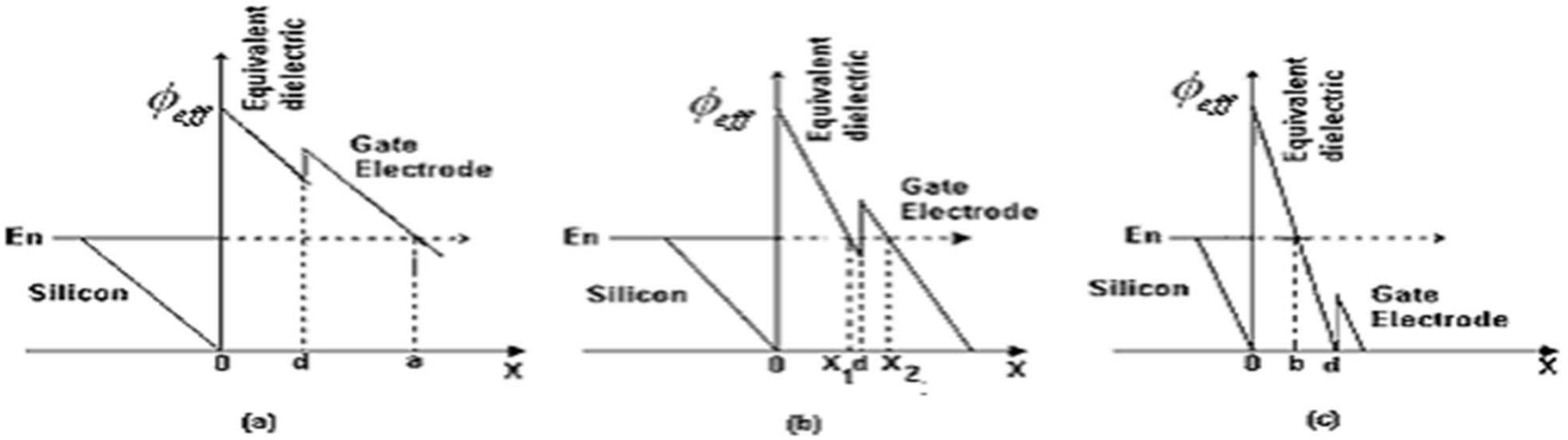
Write Mechanism: Fowler – Nordheim Tunneling



- High Applied Gate voltage → Fowler-Nordheim tunneling
- The barrier becomes Triangular in shape
- Applied gate voltage $V > \left(\phi_{eff} - E_0\right)/q$
- Electrons tunnel from the conduction band of Si to conduction band of oxide through part of potential barrier

Band diagram of Fowler-Nordheim tunneling

Band Structure of Tunneling under Different Conditions of Applied Electric Field



Band bending at applied electric fields under different conditions (a) $F_{eff}d \ < \phi_{eff} - E_n$

(b) $\phi_{eff} - E_n < F_{eff}d \ < \phi - E_n$ (c) $F_{eff}d \ > \phi - E_n$

F-N Tunneling Probabilty

Case I : $qF_{eff}\,d < \left(\phi_{eff} - E_o\right)$

$$D\left(E_0\right) = \exp\left(-\frac{4\sqrt{2m_{eff}}}{3q\hbar F_{eff}} \left[\left(\phi_{eff} - E_0\right)^{3/2} - \left(\phi_{eff} - E_0 - qF_{eff}\,d\right)^{3/2} \right] - \frac{4\sqrt{2m}}{3q\hbar F} \left(\phi - E_0 - qF_{eff}\,d\right)^{3/2} \right)$$

Case II : $\left(\phi_{eff} - E_o\right) < qF_{eff}\,d < \left(\phi - E_o\right)$

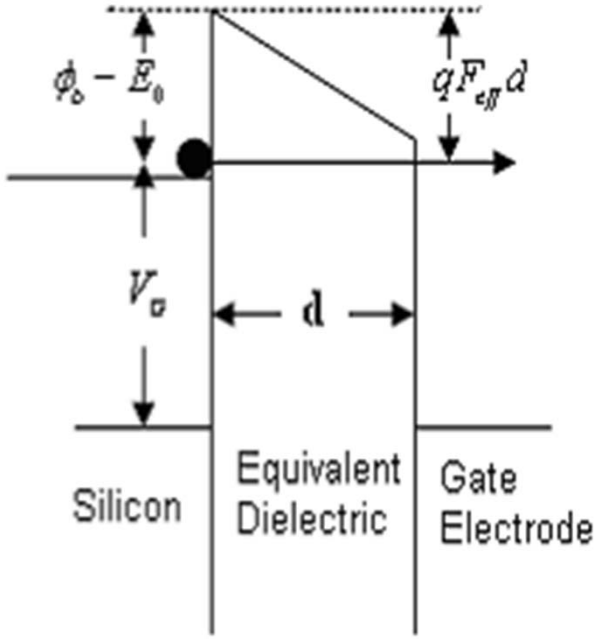
$$D\left(E_0\right) = \left\{ \sin^2\theta_2 \cosh^2(\theta_3 - \theta_1) + \cos^2\theta_2 \cosh^2\left[\theta_3 + \theta_1 + \ln(4)\right] \right\}^{-1}$$

$$\hbar\theta_i = \int_{x_{i-1}}^{x_i} \left\{ 2m^* \left| \left[V(x) - E_0 \right] \right| \right\}^{1/2} dx$$

Case III : $qF_{eff}\,d > \left(\phi - E_o\right)$

$$D(E_0) = \exp\left(-\frac{4\sqrt{2m_{eff}}}{3q\hbar F_{eff}} \left(\phi_{eff} - E_0\right)^{3/2} \right)$$

Leakage: Direct Tunneling



- Low Applied Gate voltage → Direct tunneling
- Applied gate voltage condition
- The Barrier becomes Trapezoidal in s $V < \left(\phi_{eff} - E_0\right)/q$
- Electrons tunnel directly from Si conduction band to metal instead of through oxide conduction band

Band diagram for direct tunneling

$$J_D = \frac{\left\{2m_{eff}\left(\phi_{eff} - E_0\right)\right\}^{1/2} \alpha q^2 V}{\hbar^2 d} \exp\left(\frac{2\alpha\sqrt{2m_{eff}\left(\phi_{eff} - E_0\right)}}{\hbar} d\right)$$

Parameters changed due to inclusion of Nanoparticles

- Dielectric constant of SiO_2 embedded with nc-Si determined by using Maxwell-Garnett Effective Medium Approximation (EMA)

$$\in_{nc-ox} = \frac{\in_{ox}\left\{2\nu\left(\in_{nc} - \in_{ox}\right) + \left(\in_{nc} + 2\in_{ox}\right)\right\}}{\in_{nc} + 2\in_{ox} - \nu\left(\in_{nc} - \in_{ox}\right)} \qquad \in_{eff} = \left\{\frac{t_{ox}}{\in_{ox} \cdot t} + \frac{t - t_{ox}}{\in_{nc-ox} \cdot t}\right\}^{-1}$$

- Band gap energy has been modified

$$E_{gnc} = E_{bulk} + \frac{\hbar^2 \pi^2}{2R^2}\left(\frac{1}{m_h^*} + \frac{1}{m_e^*}\right)$$

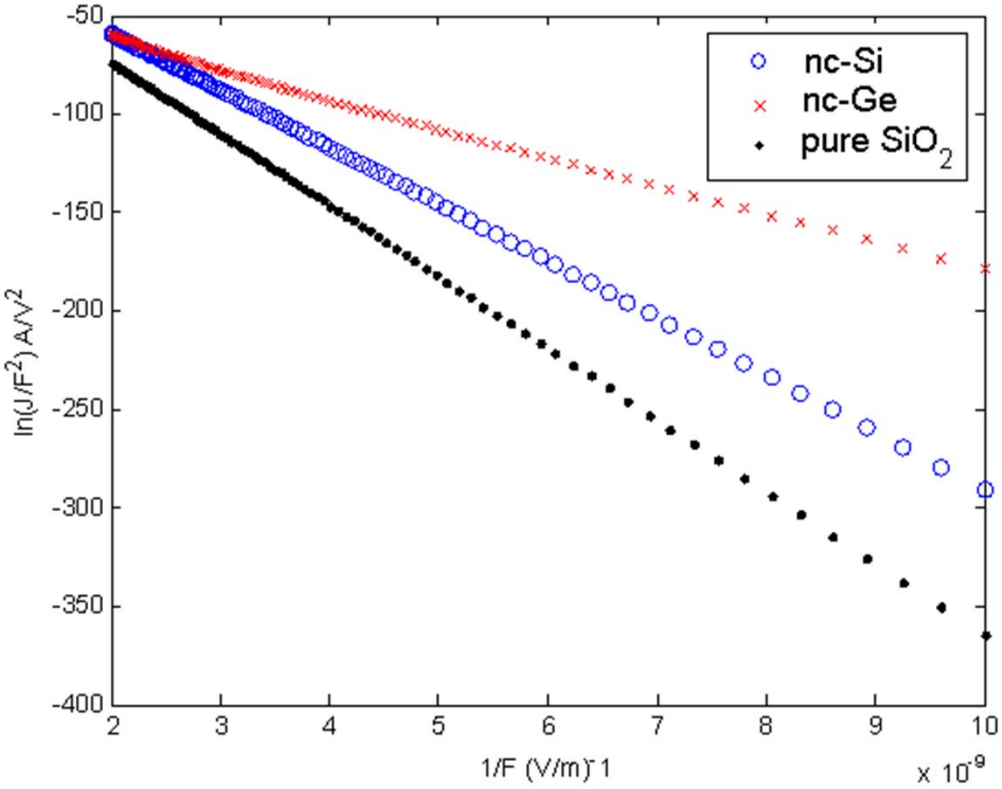
- Effective barrier height modified

$$\phi_{eff} = \frac{1}{2}\left[\frac{E_{gsio2}}{2} + \frac{1}{2}\left(E_{gsio2} \cdot (1-\nu) + \nu \cdot E_{gnc}\right) - E_{gsi}\right]$$

- Electron effective mass has been changed

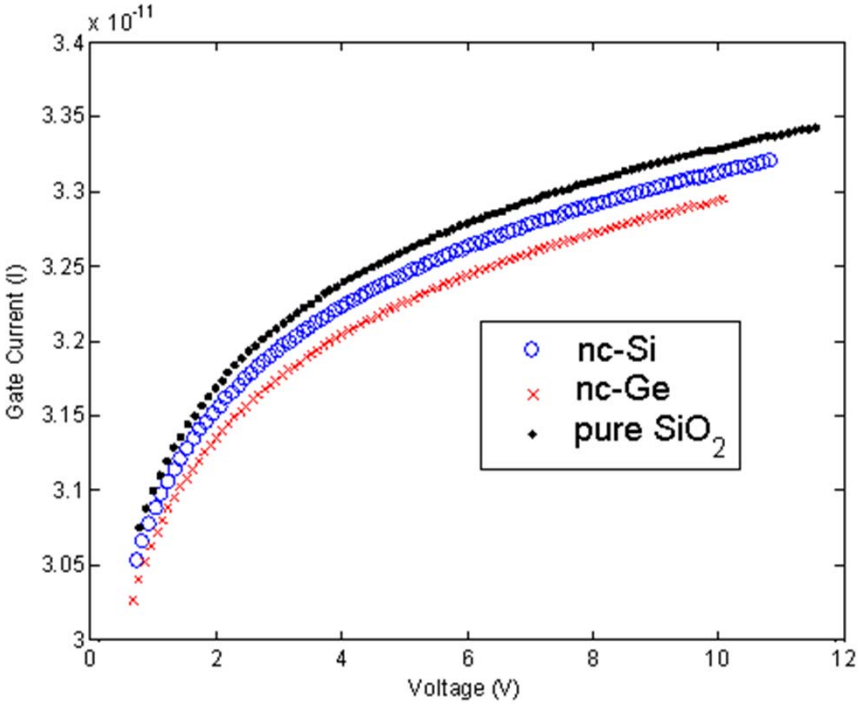
$$m_{eff} = \left[\frac{m_{sio2} d_{sio2}}{d} + \frac{m_{nc}(d - d_{sio2})}{d}\right]$$

Simulated Fowler-Nordheim Plot



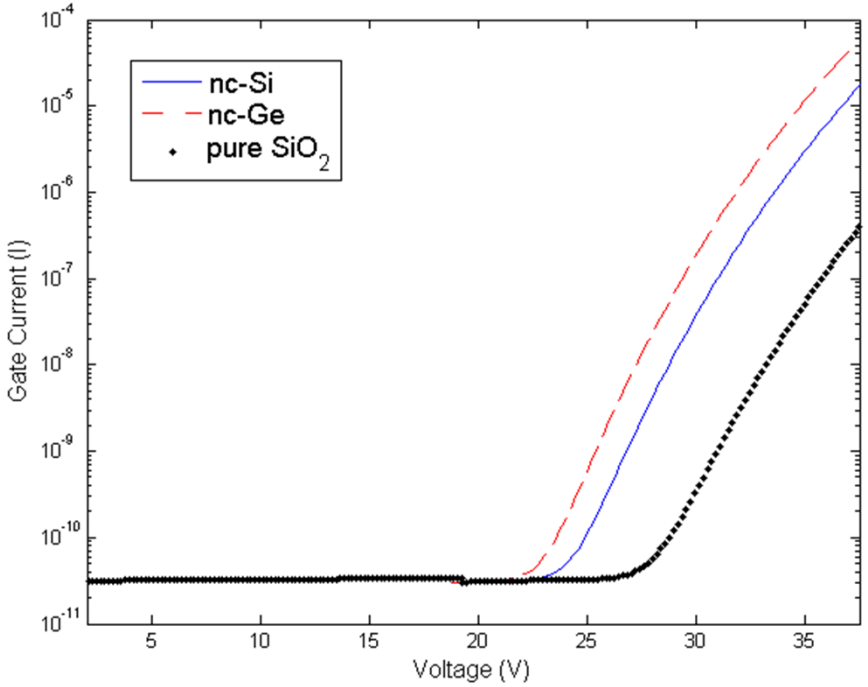
- FN plot compares the pure SiO_2 gate dielectric with the nc-Si and the nc-Ge embedded dielectric.
- Both The nanoparticles embedded composite gate dieletrics show higher F-N tunneling current density than the pure SiO_2 dielectric.
- The F-N tunneling current density is higher in nc-Ge embedded gate dielectric than the nc-Si embedded one.

Simulated Leakage Current



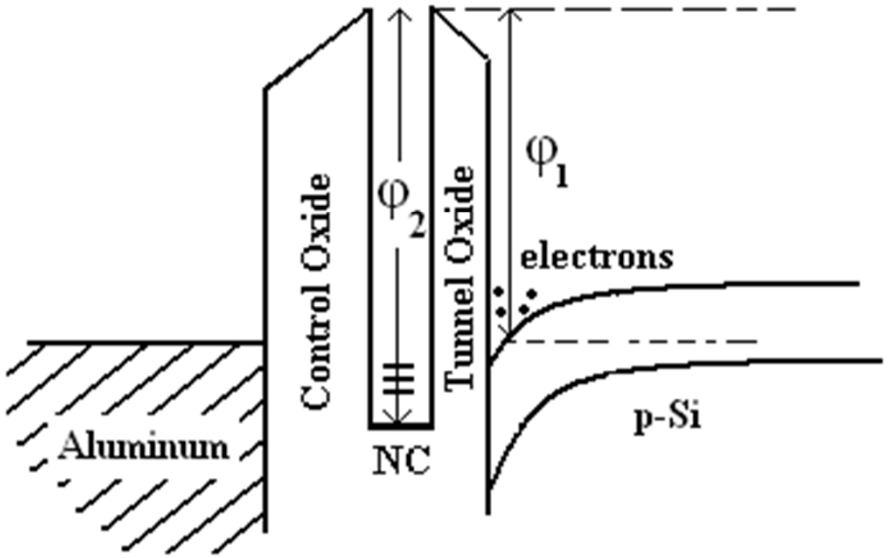
- Here it is seen that the incorporation of nanocrystals in the gate oxide somewhat reduces the direct tunneling (leakage) current compared to pure SiO_2 gate. Also it is evident that for the nc-Ge the value of the direct Tunneling current is the least.

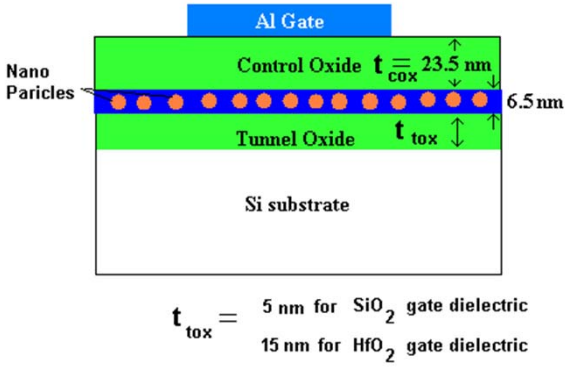
Simulated I-V Characteristics



- Nanocrystalline particles embedded gate oxide has an F-N tunneling current few decades greater compared to pure SiO_2 gate.
- Nanocrystal incorporation markedly reduces the onset voltage of F-N tunneling by ~5V-7V Volts.
- The composite gate dielectric with nc-Ge has a slightly lower value of onset voltage for F-N tunneling compared to the nc-Si embedded one.

Modified Floating Gate Approach





Charging of NCs

$$\varphi_1 = \varphi_{10} - \alpha E_{ox}^{1/2} - \beta E_{ox}^{2/3}$$

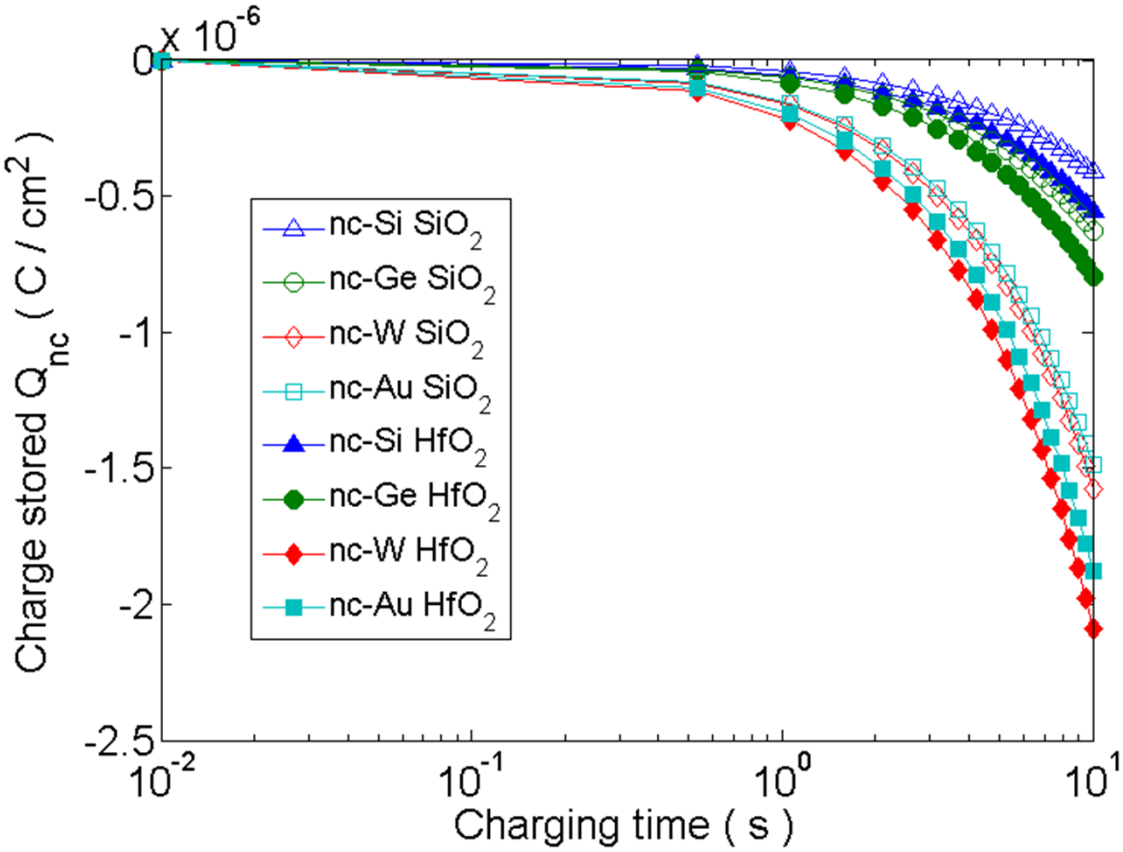
$$J_{FN} = \left(\frac{q^3 m_{si}}{16\pi^2 m_{ox}\hbar}\right)\cdot\frac{E_{tox}^2}{\varphi_1}\cdot\exp\left\{-\left(\frac{2\sqrt{8m_{ox}q}}{3\hbar}\right)\frac{\varphi_1^{3/2}}{E_{tox}}\right\}$$

Leakage from NC to Si

$$\varphi_2 = \varphi_{20} - \alpha E_{ncox}^{1/2}$$

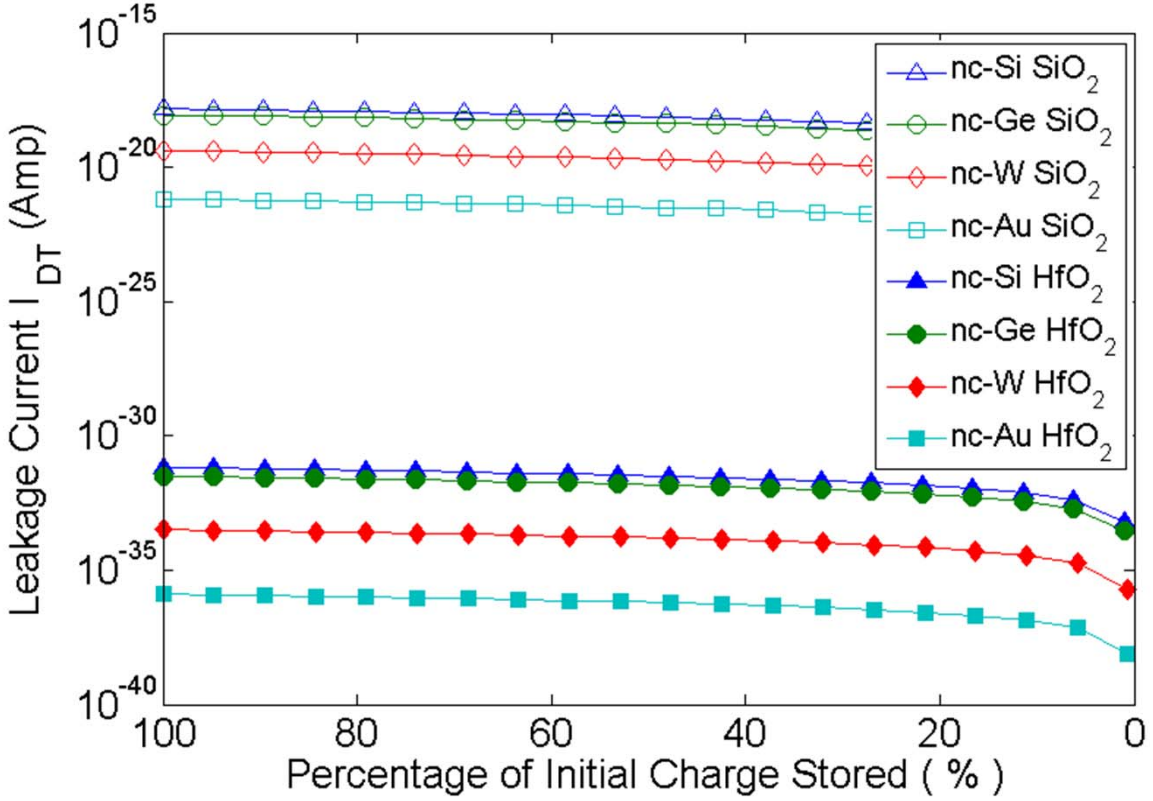
$$J'_{DT} = \frac{\left\{2m_{ox}\left(\varphi_2 - \varepsilon_{nc}\right)\right\}^{1/2}\alpha q^2 E_{ncox}}{\hbar^2}\exp\left(\frac{2\alpha\sqrt{2m_{ox}\left(\varphi_2 - \varepsilon_{nc}\right)}}{\hbar}t_{tox}\right)$$

Charge Storage of ncs



•Metal Nanocrystals store higher amount of charge.

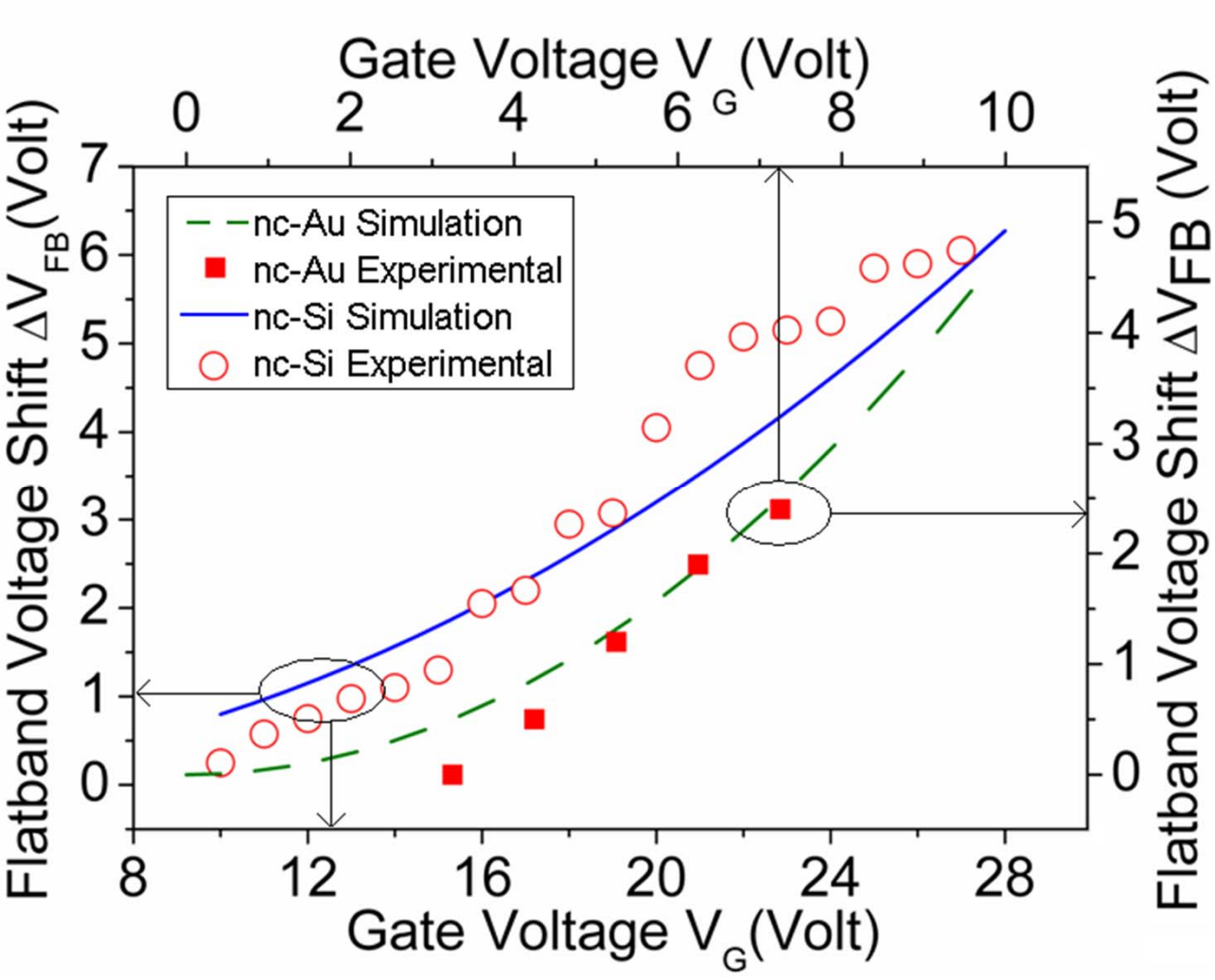
Simulated Leakage currents



•Metal Nanocrystals offer lesser leakage current compared to Semiconductor ncs.

• Use of High-k dielectrics can further reduce leakage current.

Flatband Voltage Shift



Conclusions

- MOS NVM devices are extensively used in flash memory based gadgets and computers.
- Floating Gate MOS memory elements mostly employed in flash memory devices.
- Conventional Floating Gate MOS NVMs suffer from leakage, also write voltages need to be lowered.
- Nanocrystals embedded Floating Gate MOS devices apply nanotechnology to improve device performance.
- Nc embedded MOS NVMs show lesser leakage current and lower write voltages compared to conventional MOS NVMs.
- Metal ncs and High-k dielectrics can improve the situation further.
- Nc embedded MOS NVMs may be the memory device of choice in near future.

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